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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,193	03/27/2001	Masahiko Tsuchiya	108097	9085

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EXAMINER	
TRA, ANH QUAN	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/817,193	Applicant(s) TSUCHIYA, MASAHIKO
	Examiner Quan Tra	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed 08/26/2002. Applicant's arguments have been fully considered ~~but they are not persuasive in view of~~ A new ground rejection. is applied as necessitated by amendment

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Andrews (Class AB Unity Gain Buffer Amplifier for CMOS Technology, Applicant submitted IDS).

Andrews discloses in figures 1 a differential amplifier comprising: a first differential amplifier circuit (P3, N1, N2) having a first differential pair (N1, N2) and operating based on a common input voltage (In); and a second differential amplifier circuit (N3, P1, P2) having a second differential pair (P1, P2) and operating based on the common input voltage; a third transistor (P4) of the primary conductive type which operating based on a first signal from the first differential amplifier; and a third transistor (N4) of the secondary conductive type connected to the third transistor of the primary conductive type and operating based on a second signal from the second differential amplifier circuit, wherein at least one of the first differential pair and the second differential pair is formed from a pair of transistors having a driving ability difference therebetween (column 1, third paragraph)., wherein the first differential amplifier circuit outputs the first signal in order to output a first output voltage (Vout at time from 0 to 0.5 mS, figure 2)

lower than the common input voltage though the third transistor of the primary conductive type, and wherein the second differential amplifier circuit outputs the second signal in order to output a first output voltage (Vout at time form .05 mS to 1.0 mS) higher than the common input voltage through the third transistor of the secondary conductive type.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saller et al. (USP 4757275) (newly cited) in view of Shulman (USP 6064258) (previously cited).

As to claims 1 and 7-9, Saller et al. shows in figures 3 a differential amplifier comprising: a first differential amplifier circuit (15, 16, 19, 33) having a first differential pair (15, 16, column 7, line 15-20 teaches the transistors can be FET) and operating based on a common input voltage (Vin); and a second differential amplifier circuit (17, 18, 20, 34) having a second differential pair (17, 18) and operating based on the common input voltage; a third transistor (21) of the primary conductive type which operating based on a first signal from the first differential amplifier; and a third transistor (22) of the secondary conductive type connected to the third transistor of the primary conductive type and operating based on a second signal from the second differential amplifier circuit. Thus, figure 3 shows all limitations of the claims except for at least one of the first differential pair and the second differential pair is formed from a pair of transistors having a driving ability difference therebetween. However, Shulman teaches in

column 5 that the size of transistors in differential pair can be different in order to have off-set for the amplifier. Thus, it would have been obvious to one having ordinary skill in the art to make the size of transistors in Saller et al.'s differential pair to be different for the purpose of having off-set for the amplifier. If one designs the size of Saller et al.'s transistors 16 and 18 are greater than the size of transistors 15 and 17, it is inherent for the first differential amplifier circuit outputs the first signal in order to output a first output voltage lower than the common input voltage though the third transistor of the primary conductive type, and wherein the second differential amplifier circuit outputs the second signal in order to output a first output voltage higher than the common input voltage through the third transistor of the secondary conductive type.

As to claim 2, Saller et al.'s figure 3 shows a first current mirror circuit (33) provided in the first differential amplifier circuit and formed from a first transistor of a primary conductive type and a second transistor of the primary conductive type (inherent); a second current mirror circuit (34) provided in the second differential amplifier circuit and formed from a first transistor of a secondary conductive type and a second transistor of the secondary conductive type (inherent).

As to claim 3, Saller et al.'s figure 3 shows a fourth transistor (15) of the secondary conductive type connected in series to the first transistor of the primary conductive type; and a fifth transistor (16) of the secondary conductive type connected in series to the second transistor of the primary conductive type and having a driving ability different from the fourth transistor of the secondary conductive type (teachesin Shulman's column 5, lines 7-38), wherein the fourth

transistor of the secondary conductive type and the fifth transistor of the secondary conductive type form the first differential pair.

As to claim 4, Shulman teaches the with of the fourth and fifth transistors are adjusted to obtain the design current mismatch between the transistors. In Seller et al., it is seen as an obvious design choice for selecting a driving ability of the fifth transistor of the secondary conductive type is set to be greater than a driving ability of the fourth transistor of the secondary conductive type dependent upon particular environment of use to ensure optimum performance.

As to claim 5, Saller et al.'s figure 3 shows the second differential amplifier circuit includes: a fourth transistor (17) of the primary conductive type connected in series to the first transistor of the secondary conductive type; and a fifth transistor (18) of the primary conductive type connected in series to the second transistor of the secondary conductive type and having a driving ability different from the fourth transistor of the primary conductive type (teaches by Shulman), wherein the fourth transistor of the primary conductive type and the fifth transistor of the primary conductive type form the second differential pair.

As to claim 6, it is seen as an obvious design choice for selecting a driving ability of the fifth transistor of the primary conductive type is set to be greater than a driving ability of the fourth transistor of the primary conductive type dependent upon particular environment of use to ensure optimum performance.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
October 3, 2002

Terry D. Cunningham
Primary Examiner